REMARKS

Applicants respectfully request reconsideration of the above-captioned application. Only claim 1 is pending, and has been amended as explained below.

In the final Office Action dated October 2, 2003, claim 1 was rejected under 35 U.S.C. § 102(b) as allegedly being clearly anticipated by the DeTroye patent (U.S. Patent No. 4,748,581). This rejection is respectfully traversed.

In the rejection, the Office suggests that "Detroye discloses a square root extraction circuit having first to mth digit calculating portion (S1-S4, see figure 2), each include a plurality of adders (FA, see figure 1) connected in series as claimed. The computation of the square root data as shown in figures 1 and 2 of Detroye can be seen as being performed by only additions by the plurality of full adders (FA), and the EXOR gates (EO1) are used to provide inputs ($q_i \hat{} q_j$) as that of the present invention to the adders."

In the Request for Reconsideration filed December 12, 2003, Applicants respectfully submitted that Figure 1 of the DeTroye patent includes a CAS (controllable add/subtract) cells that include a full adder as a component, but pointed out that the DeTroye circuit adds and subtracts and requires by four inputs a_i, b_i, c_i and p. The present invention uses only adders, rather than adders that are configured together with exclusive OR-gates that are controlled to be either adders or subtractors.

In an effort to move the application forward, Applicants have further amended claim 1 to recite that the plurality of adders include only a half adder and a full adder, and the full adder obtains only one bit of addition output and one bit of carry output based only on two bits of data input and one of carry input. This can be seen based

on the arrowed lines of Figure 2 of the present application, for instance, and the text related thereto, for instance.

In contrast, circuit BOA illustrated in Figure 1 of the DeTroye patent has four inputs (data inputs a_i and b_i, carry input c_i and a control input p) and four outputs (the data output b_i, a data carry output c_i+1 and an addition output s_i and a control output p), which makes the DeTroye patent significantly different than the presently claimed invention. It should be clear from this language that the circuit of the DeTroye patent is structurally different from the present invention.

If the circuit BOA illustrated in Figure 1 of the DeTroye patent is seen as a full adder (FM) portion and an exclusive OR-gate (E01) portioned separately, then another circuit for outputting the control input p and the data input b_i as a control output p and the data output b_i should exist. This additional circuit does not correspond to any element of the present invention such as full adders, half adders, and exclusive OR operation ($q_i \hat{} q_j$) used for providing the adder as stated by the Office. Therefore, it should also be clear that the circuit BOA shown in Figure 1 of the DeTroye patent requires such an additional circuit and is different from the plurality of adders including only full adders and half adders wherein the full adder obtains only one bit of addition output and one bit of carry output based on two bits of data input and one bit of carry input. Accordingly, it is respectfully submitted that the DeTroye patent does not disclose the present invention particularly as now recited in the detailed recitations of pending claim 1.

In light of the foregoing, Applicants respectfully request reconsideration and allowance of the above captioned application. Should any residual issues exist, the Examiner is invited to contact the undersigned at the number listed below.

Respectfully submitted,

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